

Remarks/Arguments**Claim Rejections – 35 USC 102****5 Examiner:**

Claims 1 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Beddingfield, US Patent 5,977,632.

10 Beddingfield discloses providing a semiconductor wafer (10), which comprises a substrate (10), an integrated circuit (not shown), and at least one bump pad (12) formed on the substrate and electrically connected with the integrated circuit, forming a first dielectric layer (16) on a surface of the bump pad; performing an etching process to form a contact hole in the first dielectric layer (figure 1) and to expose a portion of the bump pad (12); forming a second dielectric layer (18) on a surface of
15 the semiconductor wafer outside of the contact hole, performing an under bump metallurgy (UMB) process so as to form a metal layer (24) on a surface of the contact hole; forming a solder bump(26) on the metal layer corresponding to the contact hole; and performing a connection process to complete connection of the semiconductor wafer and a packaging board (figure 7). Please see figures 1-7 and discussion on
20 column 2, line 35 to column 4, and line 35.

Also in regards to claim 6 wherein the second dielectric layer is composed of insulating materials, such as benocyclobutene (BCB), polyimide (PI), and BBC+PI (column 3, lines 5 to 15).

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Response:

Although Beddingfield discloses making a solder bump structure, that which is disclosed by Beddingfield fails to teach the main feature of the present invention as
30 follows: "a circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump."

As a result, for the sake of emphasizing the main feature of the present invention, the applicant politely requests adding some description into claim 1 about “performing a circuit probing and a laser repair process after the
5 formation of the solder bump, and using a probing tip in the circuit probing process by electrically connecting with the solder bump”, as previously recited in claim 5. No new material has been introduced. The Examiner has stated that Beddingfield lacks this limitation.

10 However, elsewhere in this Office action and concerning claim 5, the Examiner has stated that Liu et al., US Patent 6,395,622, “discloses circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump.”

15 Although Liu et al. discloses the feature that a circuit probing and a laser repair process are performed after the formation of the solder bump, the probing tip is used to perform the circuit probing process by electrically connecting with the bump pad (Fig.3c). However, the present invention uses a probe tip electrically connected with
20 the solder bump to find invalid memory cells. Thus, the Applicant believes that not only does Liu et al. not teach the pertinent limitation, but also the present application’s inventive step provides direct and tangible improvements over the cited prior art.

Because Liu et al. connects the probe to the bump pad, Liu et al. cannot get to the
25 aim of the present invention of preventing a problem that the probing mark on the surface of the bump pad may cause the metal layer to lose or reduce its functions of providing an adhesion and diffusion barrier, because the metal layer formed on the surface of the bump pad has poor step coverage. Also, Liu et al. cannot get to the aim of the present invention of preventing a problem that a circuit probing process directly
30 performed on the bump pad may result in bare copper or cracked insulation layers because of excess probing force when an interconnect system uses a copper process and low-k materials as insulation layers.

In contrast, the present invention's method of performing circuit testing by electrically connecting with the solder bump instead of the bump pad can prevent the quality of the metal layer formed on a surface of the bump pad and the structure of electronic devices of the semiconductor wafer from being damaged by the circuit probing process. The present invention also can prevent the formation of voids resulting from the laser repair process forming trenches on the semiconductor wafer, which affects the reliability of products.

Therefore, the Applicant believes that claim 1 as amended represents a new and useful process, not taught or suggested in the prior art and respectfully requests reconsideration of claim 1.

Additionally, although Beddingfield discloses the second dielectric layer is composed of insulating materials, such as polyimide (PI). However, because claim 6 is dependent on claim 1 and Beddingfield does not teach the main feature of above-modified claim 1, Beddingfield also fails to teach the limitations of claim 6. Therefore, reconsideration of claims 6 is politely requested.

Claim Rejections – 35 USC 103

Examiner:

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beddingfield as applied to claims 1 and 6 above, and applicant's admitted prior art (AAPA).

Beddingfield is applied supra but lacks the anticipation wherein the semiconductor wafer further comprises: a plurality of fuses electrically connected with the integrated circuit; at least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key. AAPA discloses semiconductor wafer

comprises a substrate 12, which has an integrated circuit region (not shown) comprising an embedded memory array formed on its surface. The surface of the substrate 12 further comprises a bump pad 14, a plurality of fuses 16, and an alignment key 18. The bump pad 14 is electrically connected with the integrated circuit region. Therefore, after completing a subsequent packaging process, the integrated circuit is able to electrically connect to an external circuit through the bump pad 14. In view of this disclosure it would of been obvious to one of ordinary skill in the art at the time of the invention to form a plurality of fuses electrically connect with the integrated circuit; at least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key as taught by AAPA in view of the primary reference of Beddingfield, because the alignment key provides a means for visual inspection and the fuse provide electrical connection for probe testing.

Response:

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Beddingfield just discloses the solder bump structure art and method of making as taught by AAPA, but fails to teach the main feature of amended claim 1 of the present invention as follows: a circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump.

AAPA also just discloses uses a "probing tip" (not shown) electrically connected to the bump pad 14 to find invalid memory cells, word lines, or conducting wires within the embedded memory in the integrated circuit region. The AAPA also fails to teach the main feature of modified claim 1 of the present invention as follows: a circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump.

Claims 2-4 are dependent on claim 1 and the applicant has already politely requested amending claim 1 as above-mentioned to stress the feature of the present invention. Therefore, it is believed that Beddingfield and AAPA fail to teach many

of the claimed facets of this application. As a result, reconsideration of claims 2-4 is politely requested.

Claim Rejections – 35 USC 103

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Examiner:

Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beddingfield as applied to claims 1 and 6 above, and further in view of Liu et al., US Patent 6,395,622.

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Beddingfield is applied supra but lacks the anticipation of wherein the circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump. Liu discloses circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump. See figure 3c and 3d and discussion on column 3, line 30 to 60. In view of this disclosure it would have been obvious to one of ordinary skill in the art at the time of the invention to circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump as taught by Liu et al, because by testing after bumping and before laser repair the throughput is increased.

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25 Response:

Without any disclaimer regarding the merits of claim 5 as originally filed, claim 5 has been cancelled and is no longer in need of consideration.

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Claim Rejections – 35 USC 102

Examiner:

Claims 7-9 are rejected under 35 U.S.C. 102(a) as being anticipated by AAPA discloses, the semiconductor wafer 10 comprises a substrate 12, which has an integrated circuit region (not shown) comprising an embedded memory array formed on its surface. The surface of the substrate 12 further comprises a bump pad 14, a plurality of fuses 16, and an alignment key 18. The bump pad 14 is electrically connected with the integrated circuit region. Therefore, after completing a subsequent packaging process, the integrated circuit is able to electrically connect to an external circuit through the bump pad 14. The fuses 16 are formed on an upper layer of the integrated circuit region and electrically connected with the embedded memory, and after finding invalid memory cells, word lines, or conducting wires within the embedded memory by performing a circuit probing process, a laser repair process is performed to eliminate these invalid elements by cutting off the corresponding fuses.

The prior art method is first forming a first dielectric layer 20 on the surface of the semiconductor wafer 10, which completely covers the bump pad 14 and the fuses 16. The first dielectric layer 20 is also called a passivation layer and is used to seal up and to avoid moistness. Thereafter, a photo-etching-process (PEP) is performed to form a contact hole 21 in the first dielectric layer 20 above the bump pad 14 so as to expose portions of the bump pad 14. Because a subsequent laser repair process uses laser beams to penetrate and to cut off portions of the fuses 16, the first dielectric layer 20 must be composed of transparent materials. As shown in Fig.2, a circuit probing process is then performed, which uses a probing tip (not shown) electrically connected to the bump pad 14 to find invalid memory cells, word lines, or conducting wires within the embedded memory in the integrated circuit region, and the alignment key 18 is used to define the regions needed to accept laser repair. After that, an accurate laser zip process is performed to cut off portions of the fuses 16 in the regions defined by the alignment key 18 so as to destroy electrical connections of these invalid elements.

As shown in Fig.3, a second dielectric layer 22 composed of benzocyclobutene

(BCB), polyimide (PI), or BCB+PI is formed on the surface of the semiconductor wafer 10. Then, as shown in Fig.4, an under bump metallurgy (UBM) process is performed to form a metal layer 24, which is composed of specific multi-layer metal films, on a surface of the contact hole 21 by sputtering. The functions of the metal layer 24 comprise providing adhesion and diffusion barrier, improving moistness of the bump pad 14, and preventing oxidation. A solder bump 26 is then formed on the metal layer 24 corresponding to the contact hole 21 by evaporating, printing, electro-plating, dipping, or ultrasonic soldering. Finally, the semiconductor wafer 10 is placed on a packaging board (not shown), and the solder bump 26 melted by a thermal treatment.

Response:

The main difference between the present invention and AAPA is that the present invention performs a circuit probing and a laser repair process by connecting the probing tip with the solder bump after the formation of the solder bump, and AAPA performs a circuit probing and a laser repair process by connecting the probing tip with the bump pad before the formation of a solder bump.

As a result, AAPA fails to many of the claimed facets of this application. However, for the sake of emphasizing the main feature of the present invention, the applicant politely requests adding the limitations previously found in claim 10 about "a circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump" in to claim 7. No new material has been introduced.

Elsewhere in this Office action the Examiner has suggested that Liu et al., US Patent 6,395,622, the limitations added to claim 7.

As detailed in discussion of claim 1, although Liu et al. disclose the feature that a circuit probing and a laser repair process are performed after the formation of the

solder bump, the probing tip is used to perform the circuit probing process by electrically connecting with the bump pad (Fig.3c). However, the present invention uses a probe tip electrically connected with the solder bump to find invalid memory cells. Thus, the Applicant believes that not only does Liu et al. not teach the pertinent
5 limitation, but also the present application's inventive step provides direct and tangible improvements over the cited prior art.

Therefore, the Applicant believes that claim 7 as amended represents a new and useful process, not taught or suggested in the prior art alone or in combination and
10 respectfully requests reconsideration of claim 7 and claims 8-9 dependent thereon.

Claim Rejections – 35 USC 102

Examiner:

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Claims 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Loo et al, US Patent 6,118,180.

Loo discloses providing a semiconductor wafer (400), which comprises a
20 substrate, an integrated circuit, and at least one bump pad (402) formed on the substrate and electrically connected with the integrated circuit, forming a dielectric layer (406) on a surface of the pump pad; performing an etching process to form a contact hole in the dielectric layer (figure 6) and to expose a portion of the pump pad; performing an under bump metallurgy (UMB) process so as to form a metal layer (408)
25 on a surface of the contact hole; forming a solder bump (412) on the metal layer corresponding to the contact hole; and performing a connection process to complete connection of the semiconductor wafer and a packaging board. See figure 3-6 and discussion on column 5, line 30 to column 8, line 15.

30 Response:

Loo et al. fail to teach the main feature of the present invention as follows: a

circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump.

5 Therefore, for the sake of emphasizing the main feature of the present invention, the applicant politely requests to add some description about “a circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump” into claim 7. The new limitations are supported by claim 10
10 and no new material has been introduced.

 Elsewhere in this Office action and concerning claims 8 and 9, the Examiner has stated that Loo et al. lacks the anticipation of the new limitations to claim 7 but that Liu discloses circuit probing and a laser repair process are performed after the
15 formation of the solder bump, and a probing tip is used to perform the circuit probing by electrically connecting with the solder bump.

 As detailed in discussion of claim 1, although Liu et al. disclose the feature that a circuit probing and a laser repair process are performed after the formation of the
20 solder bump, the probing tip is used to perform the circuit probing process by electrically connecting with the bump pad (Fig.3c). However, the present invention uses a probe tip electrically connected with the solder bump to find invalid memory cells. Thus, the Applicant believes that not only does Liu et al. not teach the pertinent limitation, but also the present application’s inventive step provides direct and tangible
25 improvements over the cited prior art.

 Therefore, the Applicant believes that claim 7 as amended represents a new and useful process, not taught or suggested in the prior art and respectfully requests reconsideration of claim 7.

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Claim Rejections – 35 USC 103

Examiner:

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loo et al as applied to claim 7 above, and Applicant's Admitted Prior Art (AAPA).

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Loo is applied surpa but lacks the anticipation wherein the semiconductor wafer comprises: a plurality of fuses electrically connected with the integrated circuit; at least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key. AAPA discloses a semiconductor wafer 10 comprises a substrate 12, which has an integrated circuit region (not shown) comprising an embedded memory array formed on its surface. The surface of the substrate 12 further comprises a bump pad 14, a plurality of fuses 16, and an alignment key 18. The bump pad 14 is electrically connected with the integrated circuit region. Therefore, after completing a subsequent packing process, the integrated circuit is able to electrically connect to an external circuit through the bump pad 14. In view of this disclosure it would have been obvious to one of ordinary skill in the art at the time of the present invention to form a plurality of fuses electrically connected with the integrated circuit; at least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key as taught by AAPA in view of the primary reference of Loo, because the alignment key provides a means for visual inspection and the fuse provide electrical connection for probe testing.

Response:

25 Loo et al. just discloses a semiconductor flip chip die metal "layout" which provides a flat UBM where surface metal pads are narrower than UBMs in order to accommodate decreased die pitch, but does not disclose the main feature of the present invention performing a circuit probing process and a laser repair process to eliminate these invalid memory cells, word lines, or conducting wires within the embedded memory.

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Additionally, AAPA also doesn't disclose the main feature of the present

invention performing a circuit probing and a laser repair process after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump”, as recited in the amended claim 7.

5 Claims 8-9 are dependent on claim 7 and the applicant has already politely requested amending claim 7 as above-mentioned to stress on the feature of the present invention. Therefore, it is believed that Loo et al. and AAPA fail to teach many of the claimed facets of this application. As a result, reconsideration of claims 8-9 is politely requested.

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Claim Rejections – 35 USC 103

Examiner:

15 Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Loo applied to claim 7, and further in view of Liu et al., US Patent 6,395,622.

20 Loo is applied surpa but lacks the anticipation of wherein the circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump. Liu discloses circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing by electrically connecting with the solder bump. See figures 3c and 3d and discuss on column 3, line 30 to 60. In view of this disclosure it would have
25 been obvious to one of ordinary skill in the art at the time of the invention to circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump as taught by Liu et al, because by testing after bumping and before laser repair the throughput is increased.

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Response:

Without any disclaimer regarding the merits of claim 10 as originally filed, claim 10 has been cancelled and is no longer in need of consideration.

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Sincerely yours,

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